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EXAMINER	
TRIMMINGS, JOHN P	
ART UNIT	**PAPER NUMBER**
2133	8

DATE MAILED: 01/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/894,007	FOUGHT ET AL.	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/09/2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claims 1-30 are presented for examination.

Drawings

1. The drawings are objected to because FIG. 2 "stbb" appears to be named wrong. The examiner believes it should be FIG. 2 "stbn". The flip-flops 132, 134, 136, and 138 do not show the type of clock at the input; please change drawing to indicate "clk 100". Also, FIG. 2 130 is described in the specification as a Mixer, and in the drawing as a Muxing circuit. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: On page 8 line 18, reference is made to "loaden". The examiner is unsure what the quoted word means, and requests that the applicant review this sentence for clarity. Appropriate correction is required.

3. The disclosure is objected to because of the following informalities: On page 13 line 14, reference is made to "mode 312", but the examiner believes this should recite "mode 316". Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. Claim 20 recites the limitation "said second plurality of logic circuits" in lines 2 and 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 2, 3, 5, 6, 11, 12, 13, 14, 16, 17, 23, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Sine et al., U.S. Patent No. 5621739.

As per Claim 1 and 12:

Referring to FIG. 1 in Sine et al. teaches a buffer circuit (see Abstract) comprising a driver device (125) with an input device (115) to receive a 1st signal (from 110), the driver (125) receiving the 2nd signal (120) and outputting a 3rd signal, and a comparing device (130, 116) receiving the 3rd signal, producing a 4th signal (output of 130), comparing the 4th signal with the 1st signal (at 116).

As per Claim 2 and 13:

This claim is dependent on Claim 1 and 12 respectively, and in the same reference, Sine et al., FIG. 2 builds on the device of Claim 1 and 13 a circuit that allows

(column 4 lines 1-14) precise skew measurements by providing a plurality (column 4 lines 15-16) of latches (208) that receive input from the 1st multiplexor (204).

As per Claim 3 and 14:

Sine et al anticipates this claim, dependent on Claim 2 and 13 respectively, in FIG. 2 wherein a 2nd multiplexor (214) couples the latches in Claim 2 to a set of latches (220) that couple to the drivers. As specified in column 4 lines 41-46, the latch 220 is followed by a driver/receiver, not shown in FIG. 2, but specified as a Gunning Transceiver. And it is inherent to the Gunning Transceiver that the driver/receiver follows the clocked latch.

As per Claim 5 and 16:

Claims 5 and 16 limit the circuit of Claim 1 and 12 respectively, and Sine et al. completely teaches whereas the comparing device comprises a 1st plurality (see column 2 lines 54-56) of logic circuits (116) and latches (130) which output 4th signals to input of logic (116), further receiving 1st signals (from 110) and comparing the two (at 116).

As per Claim 6 and 17:

Claims 6 and 17, dependent on Claims 5 and 16 above, limit the latches to being flip-flops. The teachings of Sine et al. show clocked latches (FIG. 2) for the latch devices of Claim 5, and since it is inherent that a clocked latch is a simple form of a flip-flop circuit, Claim 6 is rejected.

As per Claim 11:

Claim 11 limits the buffer circuit of Claim 1 (FIG. 1 100), and is taught by Sine et al. in column 2 lines 54-64 as being an integrated circuit. An integrated circuit is

considered in the art as being inherently provided on a chip, which is specifically taught by Sine et al., therefore Claim 11 is rejected.

As per Claim 23:

The apparatus of Claim 1 is limited in that the 4th signal is delayed based on strobes. Sine et al. anticipates this in FIG. 2 and also in column 5 lines 29-49, where the 4th signal out of circuit 246 is based on strobe signals supplied through the Pulse Generator 248.

As per Claim 24:

Sine et al. anticipates putting the apparatus of Claim 12 (FIG. 2) on an integrated circuit (column 4 lines 15-16), therefore Claim 24 is rejected.

Claim Rejections - 35 USC § 103

a. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 4 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sine et al., U.S. Patent No. 5621739 as applied to Claims 1 and 12 above, and in view of Takeda et al., U.S. Patent No. 5805601. The two subject claims define the arrangement where data is multiplexed on a time basis using a faster clock to bring together slower clocked data into a single output. Sine et al. does not show this form of data combining. However, in an analogous art, Takeda et al. uses this very technique to combine signals being sent out of a driver device, much in the same way as is claimed by the applicant. The arrangement of Takeda uses a clock T (FIG. 5A) to multiplex data, and a clock T/3 (FIG. 5B) to demultiplex a plurality of data signals. Takeda et al., in column 2 lines 43-57 suggests that the management of large scale signal transfers is better accomplished with fewer pins and overhead using this method. Motivated by Takeda et al., one with ordinary skill in the art at the time of the invention would have combined Takeda et al. with Sine et al. in order to squeeze as much functionality as possible onto a chip. Therefore, Claims 4 and 15 are rejected.

10. Claims 7-10, 18-22, and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sine et al., U.S. Patent No. 5621739 as applied to Claims 3 and 16 above, and in view of Kobayashi et al., U.S. Patent No. 5646948.

As per Claims 7 and 18:

The logic circuits of Claims 5 and 16 are defined in these two claims as being XOR circuits. Sine et al., using a functionally similar arrangement however uses XNOR circuits. In an analogous art, in reporting comparison results, Kobayashi et al. uses XOR circuits (FIG. 2 $4X_1$) to report on comparisons (see Abstract and FIG. 10). Kobayashi et al. also suggests (column 2 lines 44-59) that the method provides effective parallel comparisons with minimum overhead. Based on the motivation of Kobayashi, as well as the comparison XOR circuit, one with ordinary skill in the art at the time of the invention would be inclined to combine the two teachings, and therefore Claims 7 and 18 are rejected.

As per Claims 8-10 and 19-21:

These claims, also dependent on Claims 5 and 16, specify that the logic output of Claims 5 and 16 comparison circuit above is connected both to an AND and an OR circuit, the outputs of which provide two signals indicating the two signals AT LEAST ONE FAIL, and ALL FAIL. Sine et al. does not teach this extension of the comparison circuit in the above claims. But, Kobayashi, in FIG. 10, OFAIL and AFAIL serve the exact same function, and are each driven by an AND and OR arrays as per Kobayashi et al. column 12 lines 2-25, which is the same as is claimed by the applicant. And, Kobayashi et al. suggests (column 2 lines 44-59) that the method provides effective

parallel comparisons with minimum overhead. Based on the motivation of Kobayashi, as well as the comparison circuit of Sine et al., one with ordinary skill in the art at the time of the invention would be inclined to combine the two teachings in order to effectively provide parallel comparisons, and therefore Claims 8-10 and 19-21 are rejected.

As per Claim 22:

This claim, dependent on Claim 21 above, which specifies the two error signals (OFAIL and AFAIL), further adds to the apparatus a device that uses the OFAIL and AFAIL signals in determining if the tested driver is bad. Sine et al., in column 8 lines 5-67, and in column 9 lines 1-40, describes a circuit (delayed strobes) and methodology of using the circuit to determine if the driver is defective, therefore, Claim 22 is rejected.

As per Claims 28-30:

Based on the method of Claim 25 below, the applicant applies the two signals of Kobayashi et al. (OFAIL and AFAIL of Claim 21 above) to a methodology that compares the time between OFAIL and AFAIL. Sine et al., in column 9 lines 20-40 performs the same function, therefore Claims 28-30 are rejected.

11. Claims 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sine et al., U.S. Patent No. 5621739, as being obvious. These claims specify the method of testing a driver circuit (see FIG. 2) based on the device of Sine et al., as rejected above, by strobing the data with two strobes, and comparing the result signals with the original signal, all on one chip. Sine et al., in column 9 lines 1-40 describes such a method, and though not worded precisely as is the applicant's claim, the method performs the same functional test. One with ordinary skill in the art at the time of the

invention, given the circuit of Sine et al., and thus the teachings of the hardware, would apply a method in such a manner as to take advantage of the device in a similar manner as the applicant has done. Therefore, Claims 25-27 are rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on weekdays, 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-2394.

Gregory J. Lamarre
for
Albert DeCady
Primary Examiner

John P Trimmings
Examiner
Art Unit 2133

jpt